IN THE CLAIMS

1-16. Cancelled

17. (Currently Amended) A non-causal channel equalization communication system, the system comprising:

a multi-threshold ~~decision~~ circuit having an input to accept a non-return to zero (NRZ) data stream, an input to accept threshold values, and outputs to provide a plurality of bit estimates for each NRZ data, responsive to a plurality of voltage threshold levels; and,

a non-causal circuit having inputs to accept the bit estimates from the multi-threshold ~~decision~~ circuit and an output to supply a first bit value for a current clock cycle in response to ~~the non-causal circuit~~ comparing a first ~~current~~ bit estimate for the current clock cycle, to bit values determined in non-current clock cycles ~~decisions made across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate determined in response to non-causal bit value comparisons~~.

18. (Currently Amended) The system of claim 17 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs to accept the bit estimates, the future decision circuit having outputs to supply [[a]] the first bit estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision

circuit comparing the first bit estimate to both the second bit value, determined for a clock cycle ~~received~~ prior to the current clock cycle ~~first bit estimate~~, and the third bit value, determined for a clock cycle ~~received~~ subsequent to the current clock cycle ~~first bit estimate~~, the present decision circuit having an output to supply [[a]] the first bit value determined in response to comparing the first bit estimate[[s]] to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

19. (Original) The system of claim 18 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the NRZ data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the NRZ data stream, an input establishing a second threshold (V0), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the NRZ data stream, an input establishing a third threshold (Vopt), and an output to provide a signal when the NRZ data stream input has an approximately equal probability of being a "0" value as a "1" value.

20. (Original) The system of claim 19 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" if both the second and third bit value are "0" values;

a first bit value of "0" if only one of the second and third bit values is a "0" value; and,

a first bit value of "0" if both the second and third bit values are a "1".

21. (Original) The system of claim 20 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" if both the second and third bit value are "1" values;

a first bit value of "1" if only one of the second and third bit values is a "1" value; and,

a first bit value of "1" if both the second and third bit values are a "0".

22. (Previously Presented) The system of claim 21 wherein the multi-threshold circuit accepts an NRZ data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply threshold values to the multi-threshold circuit in response to FEC corrections and an output to supply a stream of corrected data bits.

23. (Previously Presented) The system of claim 22 wherein the FEC circuit includes a first threshold generator having an inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the first threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "1" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values; and,

wherein the first threshold generator has an output to supply the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

24. (Previously Presented) The system of claim 23 wherein the FEC circuit includes a second threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the second threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "0" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values; and,

wherein the second threshold generator has an output to supply the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

25. (Previously Presented) The system of claim 24 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value; and,

wherein the third threshold generator has an output to supply the third threshold (Vopt) in response to corrections tracked in the first bit when one of the second or third bit values is a "1" value.

26. (Previously Presented) The system of claim 24 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator tracking the number of corrections in the first bit when the first

bit is determined to be a "1" value and adjusting the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value.

27. (Original) The system of claim 21 further comprising:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream, the first threshold generator tracking the NRZ data stream inputs when the second and third bit values both equal "1" and maintaining a long-term average of the tracked NRZ data stream inputs, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average.

28. (Original) The system of claim 27 further comprising:

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream input, the second threshold generator tracking the NRZ data stream inputs when the second and third bit values both equal "0" and maintaining a long-term average of the NRZ data stream inputs, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average.

29. (Original) The system of claim 28 further comprising:

a third threshold generator having inputs to accept the first (V1) and second (V0) thresholds, and an output to supply the third threshold (Vopt) responsive to the first and second thresholds.

30. (Original) The system of claim 29 wherein the third threshold generator supplies the third threshold approximately midway between the first and second thresholds.

31. (Original) The system of claim 28 further comprising:

a third threshold generator having an input to accept the NRZ data stream input, the third threshold generator measuring the average voltage of the NRZ data stream and supplying the third threshold (Vopt) at an output in response to the measured average.

32. (Original) The system of claim 21 wherein the multi-threshold circuit receives NRZ training data input;

wherein the non-causal circuit supplies first bit values responsive to the received NRZ training data; and,

the system further comprising:

a training circuit with a memory including predetermined training data, an input to accept the first bit values from the non-causal circuit, the training circuit comparing the received first bit values to the training data in memory, and supplying first, second, and third threshold values at an output in response to the comparisons.

33. (Currently Amended) A non-causal channel equalization communication system, the system comprising:

a multi-threshold ~~decision~~ circuit having an input to accept a data stream and outputs to provide a plurality of bit estimates for each data, responsive to a plurality of voltage threshold levels; and,

a non-causal circuit having an input to accept the bit estimates from the multi-threshold ~~decision~~ circuit and an output to supply a first bit value for a current clock cycle in response to~~, the non-causal circuit~~ comparing a first ~~current~~ bit estimate for the current clock cycle to bit values determined in non-current clock cycles ~~supplied across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate~~.

34. (Currently Amended) The system of claim 33 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply [[a]] the first bit estimate and subsequent bit values;

a present decision circuit having inputs to accept the first bit estimate, the subsequent bit values, and prior bit values, the present decision circuit comparing the first bit estimate to both the prior bit values, determined for clock cycles ~~received~~ prior to the current clock cycle ~~first bit estimate~~, and the subsequent bit values, determined for clock cycles ~~received~~ subsequent to the current clock cycle ~~first bit estimate~~, the present decision circuit having an output to supply [[a]] the first bit value determined in response to comparing the first bit estimate to the prior and subsequent bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the prior bit values.

35. (Currently Amended) A non-causal channel equalization communication system, the system comprising:

a multi-threshold ~~decision~~ circuit having an input to accept a data stream encoded with forward error correction and an output to provide a plurality of bit estimates for each data, responsive to a plurality of voltage threshold levels;

a non-causal circuit having an input to accept the bit estimates from the multi-threshold ~~decision~~ circuit and an output to supply a first bit value for a current clock cycle in response to~~, the non-causal circuit~~ comparing a first ~~current~~ bit estimate for the current clock cycle to bit values determined in non-current clock cycles ~~decisions made across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate~~; and,

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the data stream and correcting first bit values in response to the decoding, the FEC circuit having an output to supply threshold levels to the multi-threshold circuit in response to the FEC corrections.

36. (Currently Amended) The system of claim 35 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs to accept the bit estimates, the future

decision circuit having outputs to supply [[a]] the first bit estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, determined for a clock cycle ~~received~~ prior to the current clock cycle ~~first bit estimate~~, and the third bit value, determined for a clock cycle ~~received~~ subsequent to the current clock cycle ~~first bit estimate~~, the present decision circuit having an output to supply [[a]] the first bit value determined in response to comparing the first bit estimate[[s]] to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

37. (Previously Presented) The system of claim 34 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the data stream, an input establishing a second threshold (V0), and an output to supply a signal distinguishing when the data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the data stream, an input establishing a third threshold (Vopt), and an output to

provide a signal when the data stream input has an approximately equal probability of being a "0" value as a "1" value.

38. (Currently Amended) The system of claim 37 wherein the future decision circuit supplies a first bit estimate for a data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" if both the second and third bit value are "0" values;

a first bit value of "0" if only one of the second and third bit values is a "0" value; and,

a first bit value of "0" if both the second and third bit values are a "1".

39. (Previously Presented) The system of claim 38 wherein the future decision circuit supplies a first bit estimate for a data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" if both the second and third bit value are "1" values;

a first bit value of "1" if only one of the second and third bit values is a "1" value; and,

a first bit value of "1" if both the second and third bit values are a "0".

40. (Previously Presented) The system of claim 39 wherein the multi-threshold circuit accepts a data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply threshold values to the multi-threshold circuit in response to FEC corrections and an output to supply a stream of corrected data bits.

41. (Previously Presented) The system of claim 40 wherein the FEC circuit includes a first threshold generator having an inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the first threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "1" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "1" values; and,

wherein the first threshold generator has an output to supply the first threshold (V1) in response to corrections tracked when the second and third bits are both "1" values.

42. (Previously Presented) The system of claim 41 wherein the FEC circuit includes a second threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the second threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and the second and third bits are both "0" values;

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and the second and third bits are both "0" values; and,

wherein the second threshold generator has an output to supply the second threshold (V0) in response to corrections tracked when the second and third bits are both "0" values.

43. (Previously Presented) The system of claim 42 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator:

tracking the number of corrections in the first bit when the first bit is determined to be a "0" value and only one of the second and third bits is a "1" value; and,

wherein the third threshold generator has an output to supply the third threshold (Vopt) in response to corrections tracked in the first bit when one of the second or third bit values is a "1" value.

44. (Previously Presented) The system of claim 42 wherein the FEC circuit includes a third threshold generator having inputs to accept the first bit value from the non-causal circuit and the stream of corrected data bits from the FEC circuit, the third threshold generator tracking the number of corrections in the first bit when the first bit is determined to be a "1" value and adjusting the third threshold (Vopt) in response to corrections tracked when the first bit is determined to be a "1" value.

45. (Previously Presented) The system of claim 39 further comprising:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the data stream, the first threshold generator tracking the data stream inputs when the second and third bit values both equal "1" and maintaining a long-term average of the tracked data stream inputs, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average.

46. (Previously Presented) The system of claim 45 further comprising:

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the data stream input, the second threshold generator tracking the data stream inputs when the second and third bit values both equal "0" and maintaining a long-term average of the data stream inputs, the second

threshold generator having an output to supply the second threshold (V0) responsive to the long-term average.

47. (Previously Presented) The system of claim 46 further comprising:

a third threshold generator having inputs to accept the first (V1) and second (V0) thresholds, and an output to supply the third threshold (Vopt) responsive to the first and second thresholds.

48. (Previously Presented) The system of claim 47 wherein the third threshold generator supplies the third threshold approximately midway between the first and second thresholds.